10/091792
03/06/02

PATENT NUMBER and ISSUE DATE

U.S. UTILITY Patent Application

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10091792	03/06/2002	338	310 / 309	2832	Sughrue

**APPLICANTS: Huber Louis; Shoshani Ziv; 3729

**CONTINUING DATA VERIFIED:
THIS APPLICATION IS A DIV OF 09/811,844 03/19/2001

** FOREIGN APPLICATIONS VERIFIED:

PG-PUB	DO NOT PUBLISH ☐	RESCIND ☐

Foreign priority claimed	☐ yes ☐ no	ATTORNEY DOCKET NO
35 USC 119 conditions met	☐ yes ☐ no	P04870US1
Verified and Acknowledged Examiners's intials		

TITLE : Method for manufacturing a power chip resistor

U.S.DEPT. OF COMM./PAT.& TM-PTO-436L(Rev. 12-94)

NOTICE OF ALLOWANCE MAILED	Assistant Examiner	CLAIMS ALLOWED: Total Claims / Print Claim for O.G
ISSUE FEE: Amount Due / Date Paid	Primary Examiner	DRAWING: Sheets Drwg. / Figs.Drwg. / Print Fig.
☐ TERMINAL DISCLAIMER	PREPARED FOR ISSUE	Application Examiner

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